Interfacing the LTC1090 to the Z-80 MPU

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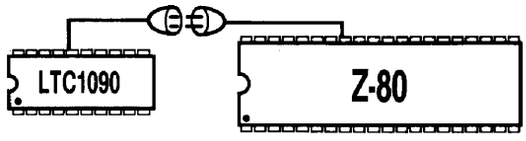

Introduction

This application note describes an interface between the LTC1090 10-bit data acquisition system and the Z-80 microcomputer. The interface is capable of completing a 10-bit conversion and shifting the data to Z-80 in 288μs. Configuration of the LTC1090 and the Z-80 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given, including data throughput rates.

Interface Details

The LTC1090 has two clock lines: ACLK and SCLK. ACLK controls the A/D conversion rate while SCLK controls the data shift rate. Data is transferred serially in a synchronous, full duplex format over D_{IN} and D_{OUT}.

The Z-80 does not have a serial port. Therefore it is necessary for the user to construct a serial port with TTL gates as shown in the schematic of Figure 1.

Hardware Description

$\overline{CS}$ is set or cleared by placing a 1 or a 0 on address line A0 and writing to an I/O port that has an even address of 128 or higher. The LTC1090 SCLK is generated by reading from an I/O port that has an address greater than 128. Data is clocked into the LTC1090 one bit at a time by placing the desired bit on D7 of the Z-80 and writing to any memory location. The serial data output of the LTC1090 is fed into D0 of the Z-80 through the 74LS126. The 74LS126 prevents the LTC1090 from writing to the data bus of the Z-80 except when the microprocessor requires data from the A/D. The ACLK of the LTC1090 is also the clock for the Z-80.

The code for this interface was developed on a Multitech MPF-1 single board development system.

The timing diagram of Figure 2 was obtained with an HP1631A logic analyzer. The Z-80 clock rate was 1.79MHz. Using a Z-80B and running it at a 6MHz clock rate, it is possible to reduce this time to approximately 100μs. This would require generating ACLK externally or dividing down the ϕ signal.

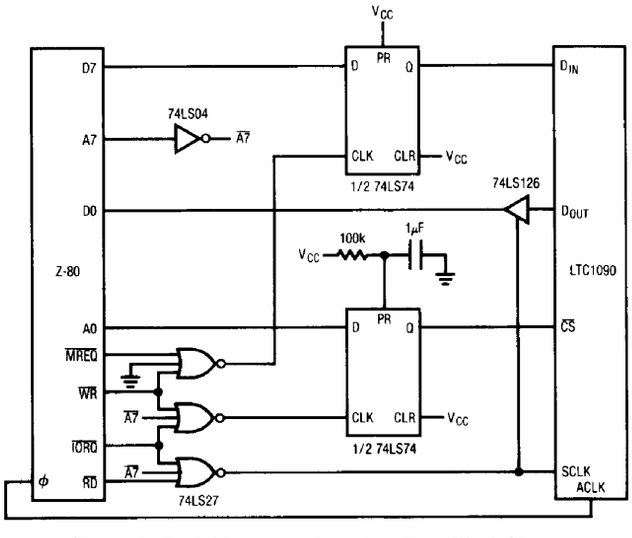

Figure 1. Serial Interface Requires Four 74LS Chips

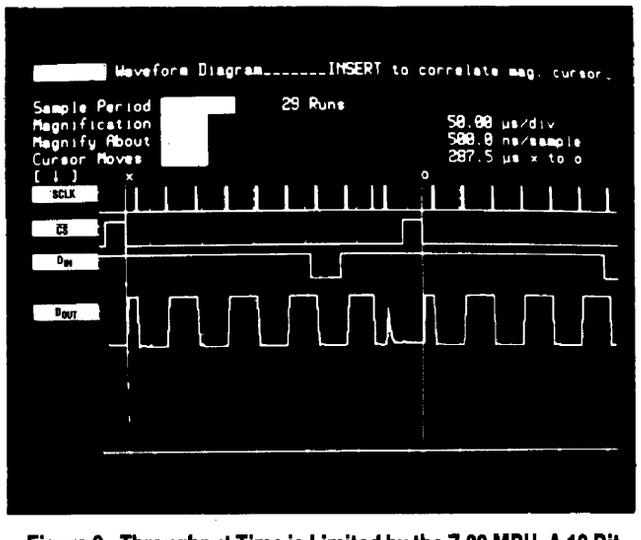

Figure 2. Throughput Time is Limited by the Z-80 MPU. A 10 Bit Conversion Result is Transmitted Every 288μs.

The analog section of the schematic of Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1090 please see the data sheet.

Software Description

The software serially shifts the D_{IN} configuration word to the LTC1090 while simultaneously reading the previous data back. Additionally, the software waits while the LTC1090 performs its next conversion before attempting the next data exchange cycle.

The code, Figure 5, first clears the C register. Next the E register, which is used as a counter, is loaded with the value 8. The D register is loaded with the D_{IN} word for the LTC1090. This word as shown in Figure 3 configures the LTC1090 for channel 7 with respect to common. D_{IN} also sets up the LTC1090 for unipolar mode, MSB first and tells the A/D to shift out 10 bits of data. $\overline{CS}$ is brought low by writing to I/O port 128 (80H). The MSB of the D register containing the D_{IN} word is then output on bit 7 of the data bus of the Z-80. The first bit of the LTC1090 D_{OUT} word is then read into the A register. The act of reading this bit also generates an SCLK pulse. The D_{OUT} bit is then shifted into the carry bit and from there it is rotated into the LSB of the B register. The next bit of the D_{IN} word is shifted into the MSB of the D register. The E register counter is decremented. At this point a test is made to determine if the first eight bits have been shifted. If not, another D_{IN} bit is output and D_{OUT} bit is read until eight bits have been shifted. The two LSBs of the D_{OUT} word are similarly shifted into the C register. These two bits are then shifted right through the carry until they are in the two MSB positions of the C register. $\overline{CS}$ is then brought high. The 10 bit LTC1090 D_{OUT} word is stored left justified in the Z-80 at this time as shown in Figure 4.

After the last SCLK pulse is ended 44 ACLK cycles must be allowed for the LTC1090 to perform the desired the A/D conversion. During this time $\overline{CS}$ is taken high. The software must ensure that this occurs.

Summary

An interface between the LTC1090 10 bit data acquisition system and the Z-80 microprocessor with a combined data conversion and transfer time of 288μs was demonstrated. The interface used four 74LS chips to interface the two devices. The 10 data bits of the LTC1090 are shifted MSB first one bit at a time. The data is stored left justified in the Z-80's internal registers.

1	1	1	1	1	1	0	1
S/D	O/S	S1	S2	UNI	MSBF	WL1	WL0

Figure 3. D_{IN} Word for LTC1090 Stored in D Register of Z-80

MSB

9	8	7	6	5	4	3	2	REG B

LSB

1	0	FILLED WITH 0's	REG C

D_{OUT} from LTC1090 stored in Z-80 registers

Figure 4. Memory Map of Z-80

LABEL	MNEMONIC		COMMENTS
BEGIN	LD	C,00H	INITIALIZE REG C
	LD	E,08H	INITIALIZE REG E
	LD	D,FDH	PUT D_{IN} IN REG D
	OUT	(80H),A	$\overline{CS}$ GOES LOW
LOOP	LD	(HL),D	OUTPUT D_{IN} BIT
	IN	A,(80H)	READ D_{OUT} BIT
	RRA		SHIFT DATA TO CARRY
	RL	B	SHIFT DATA TO REG B
	RLC	D	SHIFT D_{IN} WORD LEFT
	DEC	E	DECREMENT COUNTER
	JP	NZ,LOOP	GET NEXT BIT IF NOT 0
	IN	A,(80H)	READ BIT 1 OF D_{OUT}
	RRA		SHIFT BIT INTO CARRY
	RL	C	SHIFT DATA TO REG C
	IN	A,(80H)	READ BIT 0 OF D_{OUT}
	RRA		SHIFT BIT INTO CARRY
	RR	C	REG C SHIFTS RIGHT
	RR	C	REG C SHIFTS RIGHT
	OUT	(81H),A	$\overline{CS}$ GOES HIGH

Figure 5. Z-80 Code